REMARKS

This application has been further reviewed in light of the Office Action dated March 8, 2007. Claims 1 to 12 and 14 to 16 remain pending in the application. Claims 1, 5, 6, 10, 14 and 15 are the independent claims herein. Reconsideration and further examination are respectfully requested.

Claims 1, 2, 4, 6, 7 and 14 were rejected under 35 U.S.C. § 102(b) over U.S. Patent No. 5,961,616 (Wakasugi), Claims 3, 5, 8 and 10 were rejected under 35 U.S.C. § 103(a) over Wakasugi in view of U.S. Patent No. 5,818,603 (Motoyama), Claims 15 and 16 were rejected under § 103(a) over U.S. Patent No. 5,831,683 (Matsumoto) in view of Wakasugi, Claim 9 was rejected under § 103(a) over Wakasugi in view of U.S. Patent No. 6,175,603 (Chapman), and Claims 11 and 12 were rejected under § 103(a) over Wakasugi in view of U.S. Patent No. 6,453,272 (Slechta). Reconsideration and withdrawal of the rejections are respectfully requested.

The present invention relates to an interface apparatus (e.g., in a printer) fetching and outputting information input from an external apparatus. According to the invention, when information is input from the external apparatus, and a change is detected in the input information, the input information is fetched from the external apparatus. Then, a determination is made whether or not the fetched information is the same as information fetched a previous time. If not, then the information is fetched. If so, the fetched information is output (printed).

Referring specifically to the claims, amended independent Claim 1 is directed to an interface apparatus for inputting information from an external apparatus, comprising, a first circuit for, in accordance with a change in information input from the

external apparatus, fetching information input from the external apparatus, after an elapse of a predetermined time, and a second circuit for determining whether the information fetched by the first circuit is the same as information fetched by the first circuit a previous time, and in accordance with a determination that the information fetched by the first circuit is not the same as the information fetched by the first circuit the previous time, outputting the fetched information, and wherein, in accordance with a determination that the information fetched by the first circuit is the same as the information fetched by the first circuit the previous time, the second circuit does not output the fetched information.

Independent Claims 5, 6 and 10 are directed to a printer, a method, and a printing method, respectively, and substantially correspond to Claim 1.

Independent Claim 14 includes features along the lines of Claim 1, but is more specifically directed to an interface apparatus for inputting information from an external apparatus, comprising, a change detector for detecting a change in information input from the external apparatus and outputting a reset upon the detection of the change, a timer for inputting the reset output by the change detector and outputting a trigger after an elapse of a predetermined time from the input of the reset, a latch for inputting the trigger output by the timer and fetching information input from the external apparatus upon the input of the trigger, and a logical filter for determining whether the information fetched by the latch is the same as information fetched by the latch a previous time, and in accordance with a determination that the information fetched by the latch is not the same as the information fetched by the latch the previous time, outputting the fetched information, and wherein, in accordance with a determination that the information fetched by the latch is the

same as the information fetched by the latch the previous time, the logical filter does not output the fetched information.

Independent Claim 15 also includes features along the lines of Claim 1, but is more specifically directed to an interface apparatus for inputting information from an external apparatus, comprising, a timer for timing a predetermined time, a comparator for making a comparison between a length of a low level state in information input from the external apparatus within the predetermined time timed by the timer, and a length of a high level state in the information within the predetermined time, and for outputting a low level signal if the comparison shows that the length of the low level state is longer than the length of the high level state, and outputting a high level signal if the comparison shows that the length of the high level state is longer than the length of the low level state, and a logical filter for determining whether information indicated by the signal output by the comparator is the same as information indicated by a signal output by the comparator a previous time, and in accordance with a determination that the information indicated by the signal output by the comparator is not the same as the information indicated by the signal output by the comparator the previous time, outputting the indicated information, and wherein, in accordance with a determination that the information indicated by the signal output by the comparator is the same as the information indicated by the signal output by the comparator the previous time, the logical filter does not output the indicated information.

The applied, alone or in any permissible combination, is not seen to disclose or to suggest the features of the present invention. With regard to Claims 1, 5, 6 and 10, the applied art is not seen to disclose or to suggest at least the features of fetching

information input from an external apparatus, after an elapse of a predetermined time, in accordance with a change in information input from the external apparatus, and in accordance with a determination that the information fetched is not the same as information fetched a previous time, outputting the fetched information, and in accordance with a determination that the information fetched is the same as the information fetched by the previous time, not outputting the fetched information.

Wakasugi is seen to disclose a data change detection circuit 10 inputs data of D0 to D7 and then outputs the data of D0 to D7 to a data processing unit, a sequence circuit 25 inputs a data change signal from the data change detection circuit 10 and a strobe change signal from a strobe change detection circuit 11 and then outputs an internal strobe signal to the data processing unit based on the input signals, and the data processing unit fetches the data of D0 to D7 in response to the internal strobe signal. That is, in Wakasugi, the data fetched by the data change detection circuit 10 is surely output to the data processing unit. Moreover, in Wakasugi, since the data fetched by the data processing unit is actually fetched in response to the internal strobe signal, this data is not necessarily the same as the data fetched a previous time by the data processing unit. For this reason, in Wakasugi, output of the fetched data is not limited according to a determination that the data of D0 to D7 are not the same. Thus, Claims 1 and 6 are not believed to be anticipated by Wakasugi.

Motoyama is not seen to disclose or suggest anything that, when combined with Wakasugi, would have resulted in the present invention. In Motoyama, it is first judged whether a protocol identifier exists. Then, if the protocol identifier exists, it is judged whether an actual format of subsequent data is correct, based on format data

corresponding to the relevant protocol identifier. Thus, the proposed combination of Wakasugi and Motoyama is not seen to teach the features of Claims 5 and 10.

The other art of record, namely Matsumoto, Chapman, and Slechta have been studied but are not seen to make up for the deficiencies of Wakasugi and Motoyama, and any permissible combination of the references is not seen to result in the invention of Claims 1, 5, 6 and 10.

Similar to Claims 1, 5, 6 and 10, with regard to Claim 14, the applied art is not seen to disclose or to suggest at least the feature of a latch for inputting a trigger output by a timer and fetching information input from an external apparatus upon the input of the trigger, and a logical filter for determining whether the information fetched by the latch is the same as information fetched by the latch a previous time, and in accordance with a determination that the information fetched by the latch is not the same as the information fetched by the latch the previous time, outputting the fetched information, and wherein, in accordance with a determination that the information fetched by the latch is the same as the information fetched by the latch the previous time, the logical filter does not output the fetched information.

Along the same lines, with regard to Claim 15, the applied art is not seen to disclose or to suggest at least the feature of a logical filter for determining whether information indicated by a signal output by a comparator is the same as information indicated by a signal output by the comparator a previous time, and in accordance with a determination that the information indicated by the signal output by the comparator is not the same as the information indicated by the signal output by the comparator the previous time, outputting the indicated information, and wherein, in accordance with a

determination that the information indicated by the signal output by the comparator is the same as the information indicated by the signal output by the comparator the previous time, the logical filter does not output the indicated information.

As discussed above, in Wakasugi, output of the fetched data of D0 to D7 is not limited according to a determination that the data of D0 to D7 is not same as data fetched a previous time. Motoyama, Matsumoto, Chapman and Slechta are also not seen to teach the foregoing features. Accordingly, Claims 14 and 15, as well as the claims dependent therefrom, are believed to be allowable.

No other matters having been raised, the entire application is believed to be in condition for allowance and such action is respectfully requested at the Examiner's earliest convenience.

Applicants' undersigned attorney may be reached in our Costa Mesa, California office at (714) 540-8700. All correspondence should continue to be directed to our below-listed address.

Respectfully submitted,

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